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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/724,597	11/28/2000	Peter L. Rosefield	ATI010002	7653

34456 7590 02/14/2003

TOLER & LARSON & ABEL L.L.P.
PO BOX 29567
AUSTIN, TX 78755-9567

EXAMINER
SOWARD, IDA M

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/724,597	Applicant(s) ROSEFIELD ET AL.	
	Examiner Ida M Soward	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to Applicants' response filed January 21, 2003.

Election/Restrictions

Applicant's election with traverse of Group II, claims 14-20 in Paper No. 4 is acknowledged. The traversal is on the ground(s) that the examination of all the claims does not create an undue burden on the Office. This is not found persuasive because examining both group requires separate thought processes and a separate class searches.

The requirement is still deemed proper and is therefore made FINAL.

Response to Remarks

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figures 1-3 in view of Ibnabdeljalil et al. (6,365,978 B1) and Kameda et al. (6,130,484).

Admitted Prior Art Figures 1-3 teach an apparatus comprising: semiconductor substrate having an input output (I0) ring, the I0 ring having a bond pad portion and an active buffer portion; the bond pad portion including: a first bond pad; a second set of bond pads having one or more bond pads; and a third bond pad, wherein the second set of bond pads is immediately adjacent to the first and third bond pads. Admitted Prior Art Figures 1-3 further teach the second set of bond pads including one or more bond pads. However, Admitted Prior Art Figures 1-3 fail to teach a conductive trace coupling the first bond pad to the third bond pad; a package substrate having a power portion; a first bond wire connected to the first bond pad and the power portion; a second bond wire connected to the third bond pad and the power portion, wherein one of the first bond pad and the third bond pad being connected to the active buffer portion of the I0 ring. Ibnabdeljalil et al. teach a conductive trace **64** coupling a first bond pad **65** to a third bond pad **66** (Figure 7, cols. 7-8, lines 52-67 and 1-38). Kameda et al. teaches a package substrate having a power portion; a first bond wire **7** connected to the first bond pad **5** and the power portion; a second bond wire **3a** connected to the third bond pad **11b** and the power portion, wherein one of the first bond pad and the third bond pad being connected to the active buffer portion **2** of the I0 ring (Figures 1-2, col. 3, lines 37-65). Since Admitted Prior Art Figures 1-3, Ibnabdeljalil et al. and Kameda et al. are from the same field of endeavor (bond pad semiconductor devices),

the purpose disclosed by Kameda et al. would have been recognized in the pertinent art of Admitted Prior Art Figures 1-3 and Ibnabdeljalil et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the bond pad structure of Admitted Prior Art Figures 1-3 by incorporating the bond pad structures as taught by Ibnabdeljalil et al. and Kameda et al. to improve the reliability of the integrated circuit IC (col. 4, lines 24-33).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figures 1-3, Ibnabdeljalil et al. and Kameda et al. (6,130,484) as applied to claim 14 above, and further in view of Lebby et al. (5,5543,958).

Kameda et al. further teach a first bond pad **5** and a third bond pad **4** being power pads (Figures 1-2, col. 3, lines 37-65). However, Prior Art Figures 1-3, Ibnabdeljalil et al. and Kameda et al. fail to teach a power pad coupled to a fixed voltage source. Lebby et al. teach a power pad **27** coupled to a fixed voltage source (Figure 1, col. 4, lines 42-46). Since Admitted Prior Art Figures 1-3, Ibnabdeljalil et al., Kameda et al., and Lebby et al. are from the same field of endeavor (semiconductor structures), the purpose disclosed by Lebby et al. would have been recognized in the pertinent art of Admitted Prior Art Figures 1-3, Ibnabdeljalil et al., and Kameda et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the bond pad structures as taught by Prior Art Figures 1-3, Ibnabdeljalil et al. and Kameda et al. by incorporating the power pad of Lebby et al. to

provide a structure that requires a sufficiently small amount of power to be utilized in portable electronic equipment.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figures 1-3, Ibnabdeljalil et al. and Kameda et al. (6,130,484) as applied to claim 14 above, and further in view of Ngai et al. (US 2001/0010471 A1).
Kameda et al. further teach a first bond pad **5** and a third bond pad **4** being power pads (Figures 1-2, col. 3, lines 37-65). However, Prior Art Figures 1-3, Ibnabdeljalil et al. and Kameda et al. fail to teach a fixed voltage source being one of Vdd and Vss. Ngai et al. teach a fixed voltage source being one of Vdd and Vss (page 5, paragraph [0062]). Since Admitted Prior Art Figures 1-3, Ibnabdeljalil et al., Kameda et al. and Ngai et al. are from the same field of endeavor (semiconductor structures), the purpose disclosed by Ngai et al. would have been recognized in the pertinent art of Admitted Prior Art Figures 1-3, Ibnabdeljalil et al. and Kameda et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the bond pad structures as taught by Prior Art Figures 1-3, Ibnabdeljalil et al. and Kameda et al. by incorporating the fixed voltage source of Ngai et al. to provide high performance interconnects.

Response to Arguments

Applicant's arguments with respect to claims 14-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to semiconductor bond pad structures:

Corisis et al. (US 2002/0191383 A1) Taylor et al. (US 2002/0109240 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

ims
February 6, 2003